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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,856	02/19/2004	Yasushi Inagaki	041226-0307277	2465

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/780,856	INAGAKI ET AL	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-80* is/are pending in the application.

4a) Of the above claim(s) *6-8,14,16-74 and 76-78* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,10,15,75,79 and 80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 6-8 are withdrawn from further consideration as being drawn to non-elected subject matter because claim 6 recites the limitation of "further comprising a (another) capacitor mounted on said PCB" would read on Specie III (figure 24), which is not elected in the previous response filed on 05/17/05 (the applicant is elected Specie I, figures 10-13).

Claims 76-78 are withdrawn from further consideration as being drawn to non-elected subject matter because claim 76 recites the limitation of "further comprising a (another) chip capacitor mounted on an outer layer of the insulating and conductive circuit layers" would read on Specie III (figure 24), which is not elected in the previous response filed on 05/17/05 (the applicant is elected Specie I, figures 10-13).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 9-10, and 75, 79-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sunahara (U. S. Patent 6,153,290) in view of Ehman et al. (U. S. Patent 6,021,050), and further in view of Lauffer et al. (U. S. Patent 5,027,253).

As to claims 1, 4, and 9-10, Sunahara discloses a printed circuit board as shown in figures 1-4 constituted by alternately laminating interlayer insulating layers (9, column 5, line 30) and conductive circuits (13-18, column 5, lines 34-35) on a core substrate (1, column 5, line 29) containing a capacitor (10, column 5, line 32),

the core substrate (1), containing said capacitor (10) mounted on a surface of the PCB, is constituted by providing a first substrate (2g, 3g),

a second substrate (4g-7g) having an opening (29, 4-figure 4) for containing the capacitor and a third substrate (8g) in a multilayer manner while interposing bonding plates; and a conductive pad (19a) having a through hole (the through hole containing element 13) formed on the first substrate (2g, 3g) and connected (electrical connected) to an electrode (22, 23) of the capacitor (10), a metal film (17) formed on the electrode (22) of the capacitor (10) made by copper (column 7, lines 29-34).

Sunahara does not disclose first, second, and third substrates made of resin material. Ehman shows multilayer printed circuit board (10) having three layers (12, 14, and 16) made of polyamide resin material (column 2, lines 45-49).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use resin layers as taught by Ehman to employ the PCB of Sunahara in order to provide a reliable and flexibility of the PCB.

Sunahara and Ehman do not teach the capacitor is located immediately below the IC chip.

Lauffer shows a multiplayer package (101-figure 2) comprising a capacitor (141) immediately located below an IC chip (235).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a capacitor is located immediately below an IC chip as taught by Lauffer to employ the package of Sunahara and Ehman for purpose of reducing wiring inductance and power supply noise of the package.

As to claims 2, 3, Sunahara discloses all of the limitations of the claimed invention, except for each of said first, second and third resin substrates having a core impregnated with a resin.

Ehman shows three layers (12, 14, and 16) made of epoxy resin impregnated. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use resin impregnated layers as taught by Ehman to employ the PCB of Sunahara in order to provide a coefficient of thermal expansion mismatch and flexure of the PCB.

As to claims 75, and 79-80, Sunahara discloses a printed circuit board as shown in figures 1-4 comprising a core substrate (1) comprising first, second, and third substrates (2g-3g, 4g-7g, and 8g), insulating layers (9, column 5, line 30) and conductive circuits (13-18, column 5, lines 34-35) laminated on the core substrate (1, column 5, line 29),

a second substrate (4g-7g) having an opening (29, 4-figure 4) containing a capacitor (10); and a conductive pad (19a) having a through hole (the through hole containing element 13) formed on the first substrate (2g, 3g) and connected (electrical connected) to an electrode (22, 23) of the capacitor (10), a metal film (17) formed on the electrode (22) of the capacitor (10) made by copper (column 7, lines 29-34).

Sunahara does not disclose first, second, and third substrates made of resin material. Ehman shows multilayer printed circuit board (10) having three layers (12, 14, and 16) made of polyamide resin material (column 2, lines 45-49).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use resin layers as taught by Ehman to employ the PCB of Sunahara in order to provide a reliable and flexibility of the PCB.

Sunahara and Ehman do not teach the capacitor is located immediately below the IC chip.

Lauffer shows a multiplayer package (101-figure 2) comprising a capacitor (141) immediately located below an IC chip (235).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a capacitor is located immediately below an IC chip as taught by Lauffer to employ the package of Sunahara and Ehman for purpose of reducing wiring inductance and power supply noise of the package..

3. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sanahara ('290) in view of Ehman et al. ('050), and further in view of Gorczyca et al. (U.S. Patent 5,161,093).

As to claim 15, Sunahara discloses a printed circuit board as shown in figures 1-4 constituted by alternately laminating interlayer insulating layers (9, column 5, line 30) and conductive circuits (13-18, column 5, lines 34-35) on a core substrate (1, column 5, line 29) containing a capacitor (10, column 5, line 32),

the core substrate (1), containing said capacitor (10) mounted on a surface of the PCB, is constituted by providing a first substrate (2g, 3g),

a second substrate (4g-7g) having an opening (29, 4-figure 4) for containing the capacitor and a third substrate (8g) in a multilayer manner while interposing bonding plates; and a conductive pad (19a) having a through hole (the through hole containing element 13) formed on the first substrate (2g, 3g) and connected (electrical connected) to an electrode (22, 23) of the capacitor (10).

Sunahara does not disclose first, second, and third substrates made of resin material. Ehman shows multilayer printed circuit board (10) having three layers (12, 14, and 16) made of polyamide resin material (column 2, lines 45-49).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use resin layers as taught by Ehman to employ the PCB of Sunahara in order to provide a reliable and flexibility of the PCB.

Sunahara and Ehman do not teach an insulating bonding agent being lower in a CTE than the first resin substrate. Gorczyca teaches a PCB as shown in figure 3 comprising an insulating bonding agent (15) being lower in a CTE than a CTE of a core substrate (12), see column 11, lines 22-43.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Gorczyca employed in the PCB of Sunahara and Ehman in order to provide a sufficient strength and reduce heat.

Response to Arguments

4. Applicant's arguments with respect to claims 1-10, 15, and 75-80 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues:

(a) claim 1 recites "a conductive pad..., and a via hole..." overcome the double patenting rejection. Examiner agrees.

(b) Sunahara does not disclose "a conductive pad..., and a via hole..." Examiner disagrees because it is clearly to show in figures 1 and 3 that a conductive pad (19a) formed on a first substrate (2g-3g) having a via hole (the via hole containing a conductor 13) being ***electrical connected*** to an electrode of a capacitor (10).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
January 16, 2006.

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